17659

16172

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Answer ***each*** *Section on* ***same/separate*** *answer sheet.*
(3) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(4) Figures to the ***right*** *indicate* ***full*** *marks.*
(5) Assume suitable data, ***if necessary****.*
(6) Use of Non-programmable Electronic Pocket Calculator is ***permissible****.*
(7) Mobile Phone, Pager and any other Electronic Communication devices are ***not*** *permissible in Examination Hall.*

Marks

1. A) Attempt **any three**: **12**

i) Define :
1) Asynchronous sequential circuit
2) Noise margin
3) Fan out
4) Skew.

ii) Write any two pro's and any two con's of VHDL.

iii) What do you mean by event based and cycle based simulator ?

iv) List any four features of Spartan 3 series FPGA.

B) Attempt **any one**: **6**

i) Describe the twin tub process for CMOS fabrication.

ii) Write the VHDL program to implement 4 bit adder.

2. Attempt **any four**: **16**

a) Design a sequence detector '10' using D-FF. If the sequence is valid, it gives the output z = '1' else 'z' = 0.

b) Realize the equation $y = \overline{(u + v)(w + x)}$ using CMOS logic.

c) What do you mean by enumerated data types ? Give the suitable example.

d) What do you mean by test bench ? State its applications.

e) Draw the HDL design flow for synthesis. Write the steps in the flow.

f) Compare FPGA and CPLD (any four).

P.T.O.

Marks

3. Attempt **any four** : **16**

a) What is metastability ? Give the example.

b) Compare BJT and CMOS (any four).

c) Define 1. Entity 2. Architecture in VHDL.

d) What are the different measures should be taken to write the efficient code ?

e) Draw the ASIC design flow and explain it.

4. A) Attempt **any three** : **12**

i) Draw the Moore machine and write its o/p equation.

ii) List the any four logical operators in VHDL.

iii) What do you mean by delta delay ? Give the example.

iv) Describe the following statement with syntax :

i) wait

ii) assert.

B) Attempt **any one** : **6**

i) Describe the resistance estimation of conducting material of uniform sheets with 'L' length. ' ρ ' resistivity, 'w' width and 't' thickness.

ii) Write the VHDL program to implement 8 : 3 encoder.

5. Attempt **any four** : **16**

a) Draw the state diagram and state table for 3 bit binary counter.

b) Explain with the syntax : 1. Signal 2. Variable.

c) Describe the transmission gate with neat sketch.

d) Write the VHDL program for 4 : 1 Mux.

e) Differentiate software programming language and hardware descriptive language.

f) Draw the functional block architecture of Xilinx CPLD.

6. Attempt **any four** : **16**

a) Describe the process of oxidation.

b) Define sensitivity list. State any two VHDL syntax in which sensitivity list is defined.

c) Draw the simulation cycle and label it.

d) Draw the FPGA configurable logic block with neat label.

e) Write two examples of CPLD and FPGA. Write one application of CPLD and FPGA.
